

CLAIM AMENDMENTS

This listing of claims will replace all prior versions and listings of claims.

1 1. (Currently Amended) A method of determining a maximum optimum
2 clock frequency ~~at which a~~ of an operation of a digital processing system ~~can~~
3 operate, the method comprising the steps of:

4 generating a clock signal at an initial frequency;

5 increasing said initial frequency in a step-wise manner; ~~and~~

6 determining the operation of said digital processing system ~~at~~ each of a
7 selected number of frequencies with a timing monitor, until a clock frequency
8 is identified at which said digital processing system does not operate correctly
9 within system timing constraints; ~~and~~

10 identifying ~~a~~ the maximum clock frequency ~~at which of the operation of~~
11 said digital processing system ~~can~~ operate correctly; ~~and~~
12 using the maximum clock frequency only during a run time when the
13 digital processing system is starving output signals and blocking input
14 signals.

15 wherein characterized in that: said maximum clock frequency
16 comprises ~~the~~ a frequency immediately previous to the one ~~clock frequency~~

17 identified as being one the clock frequency at which said digital processing
18 system does not operate correctly; and in that
19 a timing monitor is provided for determining whether or not said
20 processing system can operate within system timing constraints at each
21 frequency, thereby indicating whether or not said system operates correctly
22 at the respective frequency, said timing monitor monitoring at least a level of
23 input and output buffers to prevent said output buffers from being starved of
24 data while said input buffers include data that is blocked from said
25 processing system.

1 2. (Currently Amended) A method according to The method of claim 1,
2 further comprising: including the step of
3 storing the maximum frequency in a memory programmable delay
4 element.

1 3. (Currently Amended) Method of calibrating clock generation means in
2 a digital processing system The method of claim 1, further comprising:
3 periodically performing the method of claim 1 while the system is
4 running during the run time
5 , and applying the resultant maximum frequency to said clock
6 generation means.

1 4. (Currently Amended) Apparatus for determining—An apparatus that
2 determines a maximum optimum clock frequency at which of an operation of
3 a digital processing system can operate, the apparatus comprising:
4 means for generating
5 a programmable ring oscillator that generates a clock signal at an
6 initial frequency;
7 a frequency finder and selector that increases the frequency of the
8 clock signal from the initial frequency to the maximum clock frequency
9 means for increasing said frequency in a step-wise manner;
10 and means for
11 a timing monitor that determines determining the operation of said
12 digital processing system at each of a selected number of frequencies, until a
13 clock frequency is identified at which said processor digital processing system
14 does not operate ~~correctly~~, correctly within system timing constraints, and
15 thereby
16 means for identifying ~~a~~ the maximum clock frequency at which said digital
17 processing system can operate correctly;
18 wherein the maximum clock frequency is used only during a run time
19 when the digital processing system is starving output signals and blocking
20
21 characterized in that:

22 wherein said maximum clock frequency comprises the-a frequency
23 immediately previous to the one-clock frequency identified as being one-the
24 clock frequency at which said digital processing system does not operate
25 correctly; and in that

26 said means for determining the operation of said system comprises a
27 timing monitor for determining whether or not said system can operate
28 within system timing constraints at each frequency, thereby indicating
29 whether or not said system operates correctly at the respective frequency, by
30 monitoring at least a level of input and output buffers to prevent said output
31 buffers from being starved of data while said input buffers include data that
32 is blocked from said processing system.

1 5. (Currently Amended) A method of selectively changing the frequency
2 at which a digital processing system is operating, the method comprising:

3 a) determining, when said digital processing system is reset, a
4 maximum clock frequency at which said digital processing system can
5 operate within system timing constraints;

6 , determining by maintaining a level of input and output buffers to
7 prevent said output buffers from being starved of data while said input
8 buffers include data that is blocked from said processing system and
9 storing said maximum frequency;

10 b)-generating, after reset, a clock signal at a nominal frequency, less
11 than said maximum frequency, until a signal is received indicating that an
12 increased clock frequency is required;

13 e)-generating, in response to receipt of said signal, a clock signal at
14 said maximum frequency ~~for a required time only during a run time when the~~
15 digital processing system is starving output signals

16 ; and then d) once again generating a clock frequency at said nominal
17 frequency.

1 6. (Currently Amended) A method according to The method of claim 5,
2 wherein the step of determining said maximum frequency comprises further
3 comprising:

4 using a bi-section algorithm when determining the maximum clock
5 frequency

6 generating a clock signal at an initial frequency;

7 ~~increasing said frequency in a step wise manner and determining the~~
8 ~~operation of said system each of a selected number of frequencies, until a~~
9 ~~clock frequency is identified at which said processing system does not operate~~
10 ~~correctly; and~~

11 identifying a maximum clock frequency at which said system can
12 operate correctly; characterized in that:

13 said maximum clock frequency comprises the frequency immediately
14 previous to the one identified as being one at which said system does not
15 operate correctly; and in that

16 a timing monitor is provided for determining whether or not said
17 processing system can operate within system timing constraints at each
18 frequency, thereby indicating whether or not said system operates correctly
19 at the respective frequency, said timing monitor monitoring at least a level of
20 input and output buffers to prevent said output buffers from being starved of
21 data while said input buffers include data that is blocked from said
22 processing system.

1 7. (Currently Amended) An apparatus for selectively changing An apparatus
2 that selectively changes the frequency at which a digital processing system is
3 operating, the apparatus comprising:

4 i. a programmable clock generation means ring oscillator that only
5 generates a maximum clock frequency;
6 ii. an external source that generates a nominal clock frequency;
7 ii. means for determining a timing monitor that determines, when said
8 digital processing system is reset, a the maximum clock frequency at which
9 said digital processing system can operate within system timing constraints;
10 a frequency finder that detects the maximum clock frequency of the
11 programmable ring oscillator; and

12 a clock multiplexer that switches between the nominal clock frequency
13 and the maximum clock frequency, using the maximum clock frequency only
14 during a run time when the digital processing system is starving output
15 signals and blocking input signals

16 determining by maintaining a level of input and output buffers to prevent
17 said output buffers from being starved of data while said input buffers
18 include data that is blocked from said processing system and storing said
19 maximum frequency, and storing said maximum frequency; and iii. means for
20 causing said clock generation means to: a) generate, after reset, a clock
21 signal at a nominal frequency, less than said maximum frequency, until a
22 signal is received indicating that an increased clock frequency is required; b)
23 generate, in response to receipt of said signal, a clock signal at said
24 maximum frequency for a required time; and then c) once again generate a
25 clock frequency at said nominal frequency.

1 8-14. (Canceled).